**DAILY ASSESSMENT FORMAT**

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| **Date:** | **5/30/20** | **Name:** | **Sathya br** |
| **Course:** | **Logic design** | **USN:** | **4al16ec065** |
| **Topic:** | **Analysis of clocked sequential circuits**  **Digital clock design** | **Semester & Section:** | **6th semester**  **B section** |
| **Github Repository:** | **sathyabr** |  |  |

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| **FORENOON SESSION DETAILS** |
| **Image of session** |
| **Report**  **1- Timer 555: Responsible for generating the clock pulses for the counters, the**  **frequency of the output shoul be 1 hz which means 1 second for each pulse.**  **- Counters: Responsible for generating the time in BCD (Binary Coded decimal).**  **3- Decoders : Takes the BCD of the counter as input and produces 7 segment output .**  **- 7 segments : Displays the time, of course!**  **\* Seconds have 2 displays , 2 decoders and 2 counters. The same for minutes and**  **hours.The circuit works as follows :**  **555 timer produces 1 seconde pulses to the clock input of the first counter which is**  **responsible the first column of seconds, so its output will change every second.**  **The counter produces numbers from 0 to 9 in BCD form and automatically resets to 0**  **after that.**  **so the output of the first counter will count from 0 to 9 every second and that's exactly**  **what we want from it, so we are done here. let's move to the next one.**  **What do we want here?**  **First, we want the 2nd counter to start counting when the 1st one moves for 9 to 0 (that**  **makes 10 seconds!)**  **How can this be done?**  **let's check the output of the fist counter in BCD :Second, Since we have 60 seconds in the minute we want the 2nd counter to count**  **only to 5, that makes 59 seconds maximum, when it take another pulse it doesn't count**  **to 60, instead it resets itself to 0 and send a pulse to the first counter in minutes to tell**  **it to count 1 minute**  **How can this be done?**  **From the BCD code above (6: 0110) when the output is 6 the two middle bits are 1**  **(Q1,Q2),**  **So By ANDing these two bits the output will be 1, This output will be connected to the**  **reset pin of the same counter (2nd one) and the clock input of the next one(3rd).**  **When the output is 6 the AND gate output (1) will reset the same counter and its**  **outputs goes 0000 so the output of the and gate again goes to 0 (1---->0), that will**  **clock the next counter. Beautiful!**  **Notice that the output of the counters are named : Q0 , Q1 , Q2 , Q3**  **The 4th counter will be the same as the second one so we are clocking it using the**  **Most Significant Bit of the output of the previous one.**  **Again, the 5th counter is the same as the 3rd one and takes its clock from the AND**  **gate.**  **The 5th and the 6th counters are responsible for hours so they are limited to 23, and**  **resets themselves to 00 when the 5th counter is 4 and the last one is 2 (24).**  **This is done using and gate with Q2 (3rd bit) of the 5th counter as one input and Q1**  **(second bit) of the last counter as the other input, and the output of this AND gate will**  **be connected to both resets of the last 2 counters.**  **When the last counter is 0(0000) or 1(0001), Q1 which is one of the inputs to the AND**  **gate will be 0 so the output of the AND gate will be zero. when it counts to 2 this bit**  **will be 1 so the output of the and gate will depend on the the other input which is Q2**  **of the previous counter, and this bit will be zero until it reaches 4 (0100),So, the output**  **of the and gate will be 1 (0--->1) resetting both counters to 00,**  **The output of these counters are converted to 7 segment output using 7447** |

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| **Date:** | **5/30/20** | **Name:** | **Sathya br** | |
| **Course:** | **Python Core and Advanced** | **USN:** | **4al16ec065** | |
| **Topic:** | **More Programs** | **Semester & Section:** | **6th semester**  **B section** | |
| **AFTERNOON SESSION DETAILS** | | | |
| **Image of session** | | | |
| **Report**   * **Read and Display student details** * **Average of three numbers** * **Area of a circle** * **Using the math module** | | | |